SCIENCE & TECHNOLOGY POLICY INSTITUTE

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# Executive Summary

Researchers for the IDA Science and Technology Policy Institute (STPI) surveyed available concepts for implementing a photonics foundry to enable an innovative ecosystem for advanced integrated optics and electronics. The work supports an effort to establish an academic-industry-government collaborative center in the United States to advance the research, development, manufacture, and assembly of complex integrated photonic-electronic devices.

Existing domestic photonic foundry capabilities are sufficient to support a wide range of research into innovative photonic components and applications. Key gaps exist in design tools, intellectual property, packaging, testing, education materials, and funding for researchers in the form of appropriate discounts and other sources of support available to unfunded academic researchers.

To facilitate making these capabilities available in a cost-effective manner to researchers or small industrial efforts, we recommend that an ecosystem be established with initial government support. A key component of this effort would be a broker to (1) act as an intermediary between users and fabricators; (2) orchestrate the design, fabrication, packaging, and testing; and (3) develop multi-project wafer capabilities to reduce individual user costs. Maintaining this ecosystem can be expected to help close the gaps in wafer fabrication, electronic design automation, intellectual property protection, packaging, and testing.

An implemented program would likely involve parallel efforts to reduce risk and select additional technologies for broader access, which might require a higher level of funding. A successful photonic foundry program should be expected to transition towards being substantially self-sustained within 5 years by having users pay for their services. If possible, a separate effort to fund photonics R&D during the initial start-up of the photonics foundry could markedly accelerate both development of a strong user community and progress towards self-sustainment.

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## A. Introduction

In 2013, the National Research Council released a report[1] noting the importance of photonics to the U.S. economy: "it is critical that the United States take advantage of these emerging optical technologies for creating new industries and generating job growth." The objective of this project was to survey available concepts for implementing a photonics foundry to enable an innovative ecosystem for advanced integrated optics and electronics. For the purposes of this report, the term "PIC foundry" (photonics integrated circuit) includes those semiconductor fabrication facilities that in addition to processing silicon integrated circuits (ICs) have the ability and willingness to fabricate photonic circuitry on silicon substrates. Whenever this report refers to facilities that process materials, substrates, and structures that are incompatible with those of a standard silicon foundry, the report notes the difference. Current foundry fabrication services are evaluated, as are the software, design automation and simulation capabilities, and business structure needed to allow such a foundry to provide affordable access to advanced services. Key gaps are identified and form the basis for future, more detailed study of alternative models to identify a more detailed roadmap. Initial recommendations for funding and necessary elements to enable the long-term vision to be realized are provided.

The overall goal is to establish an academic-industry-government collaborative center in the United States to advance the research, development, manufacture, and assembly of complex integrated photonic-electronic devices.

## B. Photonics: An Enabling Technology

For many applications of optics, light may be considered as a high-frequency electromagnetic wave operating at frequencies extending from the infrared to visible to ultraviolet regime of the spectrum. In general, the application of optical techniques is broad and based on a wide range of devices manufactured from disparate materials. Figure 1 shows some of the range of materials used to fabricate photonic components.

The term "photonics" refers specifically to technologies for generating, transmitting, modulating, filtering, processing, switching, amplifying, attenuating, and detecting light. It is also generally used to refer to the application of light in information systems, for signal transmission, for access to storage media, in chemical and biological sensing, and in image capture and display.

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[1] National Research Council, *Optics and Photonics: Essential Technologies for Our Nation*, Washington, DC: The National Academies Press, 2013.

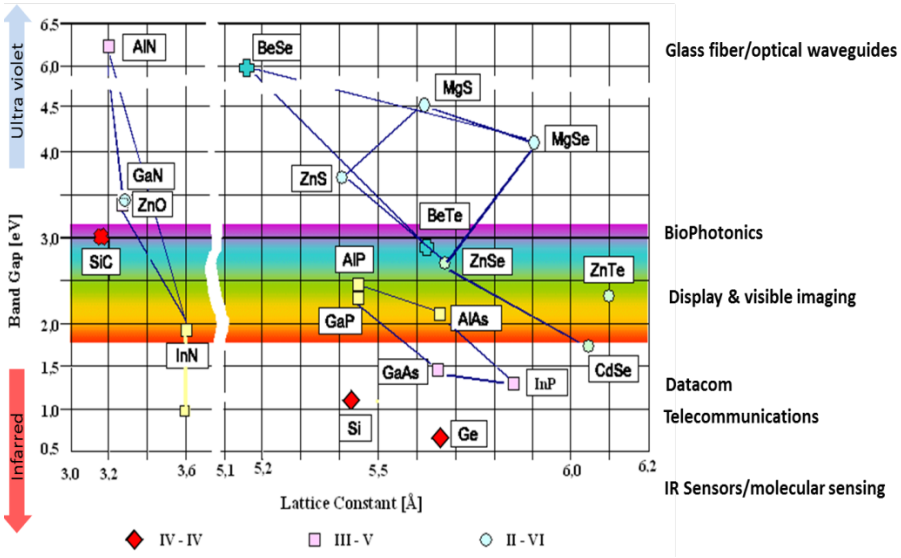



**Figure 1. Semiconductor Materials for Photonic Applications**

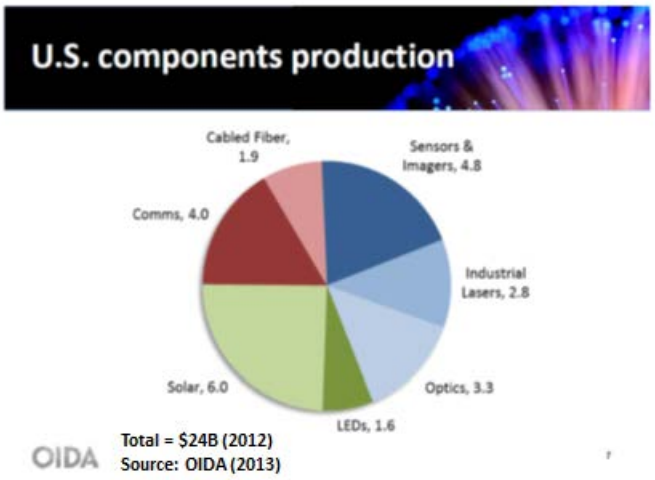
The Optoelectronics Industry Association (OIDA), an industry-based group associated with the Optical Society of America, has identified the following set of photonic market drivers:[2]

- Communications
  - Photonic integration
  - Coherent telecom transmission (100+ Gbps)
  - Software-defined networking
- Biophotonics
  - Molecular imaging, optical coherence tomography, etc.
  - Lasers for ophthalmology
  - Lasers for dermatology
  - Low-light-level therapy
  - Breathalyzers
- Photovoltaics
- Light-emitting diode lighting

[2] OIDA, *OIDA Market Update*, September 2013.

- Manufacturing
  - Fiber lasers and high-powered pump diode lasers
  - Extreme ultraviolet lighting
  - Additive manufacturing and three-dimensional (3D) printing
- Imaging and sensing
  - Gesture recognition
  - Industrial and environmental sensors
  - Low-power-diode lasers for heat-assisted magnetic recording
  - Autonomous vehicles
  - Computational imaging
  - Distributed fiber sensors
- Military
  - Mid-infrared lasers for aircraft composite materials
  - Imaging for autonomous vehicles
  - Directed-energy weapons

Photonics also has some scientific applications (including quantum computing) that may not represent large markets but are important areas for consideration of government support. In 2013 the OIDA reported that the 2012 U.S. market for photonic components is $24 billion (Figure 2) with communication applications (combined telecommunication and interconnection in data systems) contributing $4 billion of this total. The related cabled fiber (largely optical cabling used in communication systems) accounts for an additional $4.8 billion. A small fraction of the cabled fiber may include active optical cables, which incorporate photonic components into the cable connectors to allow seamless electric-to-electrical connection.




Source: OIDA, *OIDA Market Update*, September 2013.

**Figure 2. U.S. Components Production**

## 1. Photonic Integrated Circuits

Experience with microelectronic and microelectromechanical systems (MEMS) technologies has demonstrated that integration of multifunctional components during wafer-level fabrication of devices results in more reliable, more compact, more power-efficient designs which contain reduced parasitics, which in turn enable operation at higher speeds. The possibility of integration of multiple photonic—and potentially electronic and MEMS—functions with PICs fabricated on a single wafer, or in proximity, achievable using 2.5-dimensional (2.5D) or 3D integration approaches, greatly simplifies the interconnection of photonic components and is currently an active area of research and development.

## 2. Key Applications and Opportunities Driving R&D in Integrated Photonics

### a. Telecommunications

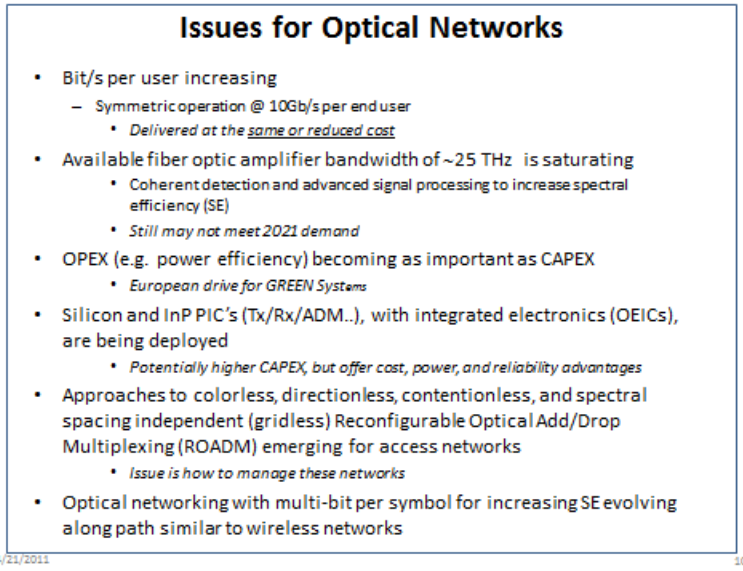
Photonic technologies are commonly used for transmission of signals in telecommunications and high-performance information-processing systems. The advantage of light for these applications is that light signals can be guided via glass or plastic fibers over significant distances with minimal losses. Most analysts believe that the growth in demand for broadband communication can be projected into the future with transmission speeds exceeding hundreds of gigabits per second, reaching terabits per second in the near future. To accommodate signals at these rates, the telecommunications industry is developing systems that rely on coherent detection of multilevel, multi-wavelength signals. Further, since the end user typically has limited data-rate requirements (0.1−10 Gbps), the

aggregation and distribution of signals within the network will require components that can rapidly reconfigure and adapt to the flow of signals through the network.

To accommodate these requirements, telecommunication networks have evolved beyond time division multiplexing of a single optical wavelength to using multiple time division multiplexing signals each carried on a different wavelength (wavelength division multiplexing). In addition, these systems are designed to operate at wavelengths matched to the very low loss transmission window of glass fiber by using components based on the indium phosphide (InP) family of materials for laser sources and detectors.

Table 1 summarizes issues related to extending the performance of these network capabilities.

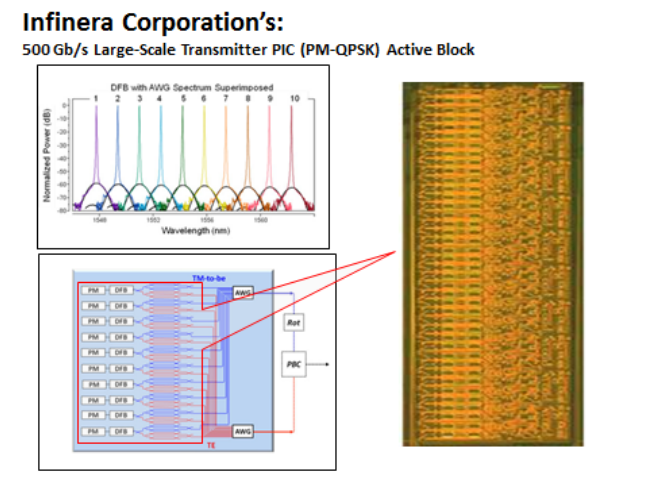
**Table 1. Issues for Optical Networks**




Source: D. Radack, R. Leheny, J. Agre, and M. Slusarczuk, *Assessment of Photonic Technologies: Interim Report to ASD*(*R&E*), IDA, April 21, 2011.

Components based on the InP compatible materials, designed to meet the high-speed and complex signal-processing requirements of advanced telecommunication transmitter and receiver modules that incorporate PIC technologies, have been developed and commercialized. Figure 3 illustrates Infinera Corporation's approach to large-scale InP PICs for high-speed optical transport. These transmitter InP PICs incorporate multiple tunable distributed feedback lasers, and nested Mach-Zehnder optical modulators for imposing a signal on each laser output and the sense and control functions required for operation of the PIC. Receiver chips incorporate local oscillator lasers and balanced detectors, and more recently reported InP PICs also incorporate complex waveguide components for on-chip signal processing and routing. (See also Infinera Corporation White Paper "Photonic Integrated Circuits: A Technology and Applications

Primer" available at www.infinera.com.) It can be anticipated that continued advances will require even more complex PICs.




Infinera Corporation's 2012 large-scale InP PIC for high-speed optical transport incorporating ten tunable distributed feedback (DFB) lasers, 20 nested Mach-Zender (MZ) modulators comprising a total of 40 Mach-Zender modulators (MZMs), and the sense and control functions required for operations of the PIC.

Source: R. F. Leheny, "Molecular Engineering to Computer Science: The Role of Photonics in the Convergence of Communications and Computing," *Proceedings of the IEEE* 100 (2012): 1475–85.

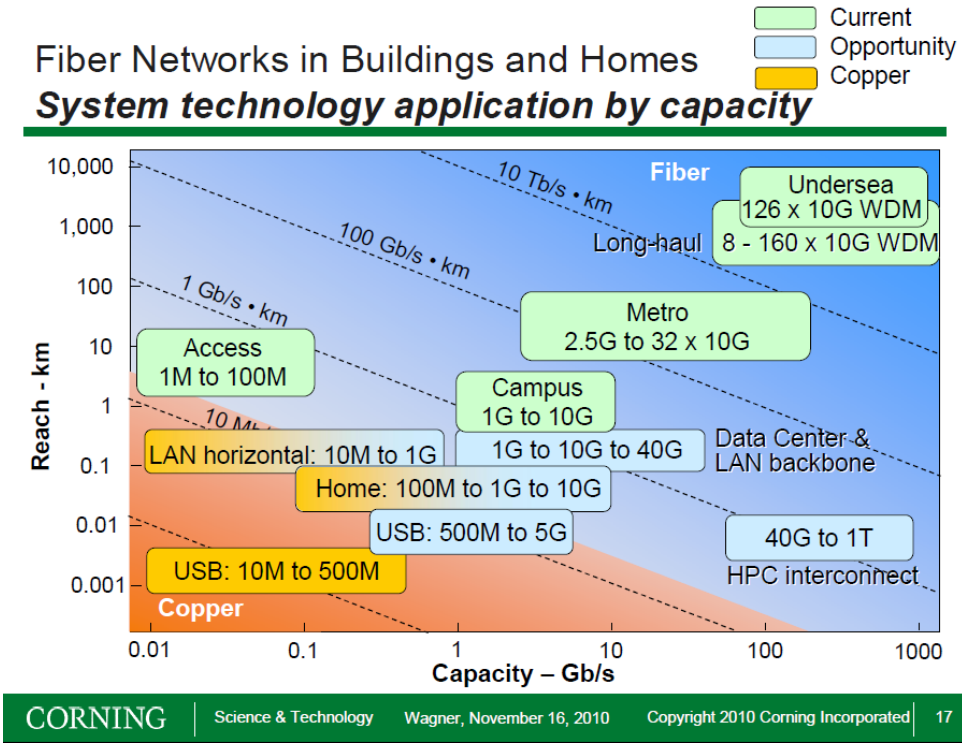
**Figure 3. Infinera PIC Technology**

### b. Interconnects in High-Performance Information Processing Systems (Data Centers and High-Performance Computing)

Over the past decade the OIDA has sponsored a number workshops and studies focused on identifying key issues related to the development of optical interconnects in high-performance information processing systems. In this section we review some of the information recently gathered by OIDA as it pertains to the need for PICs.

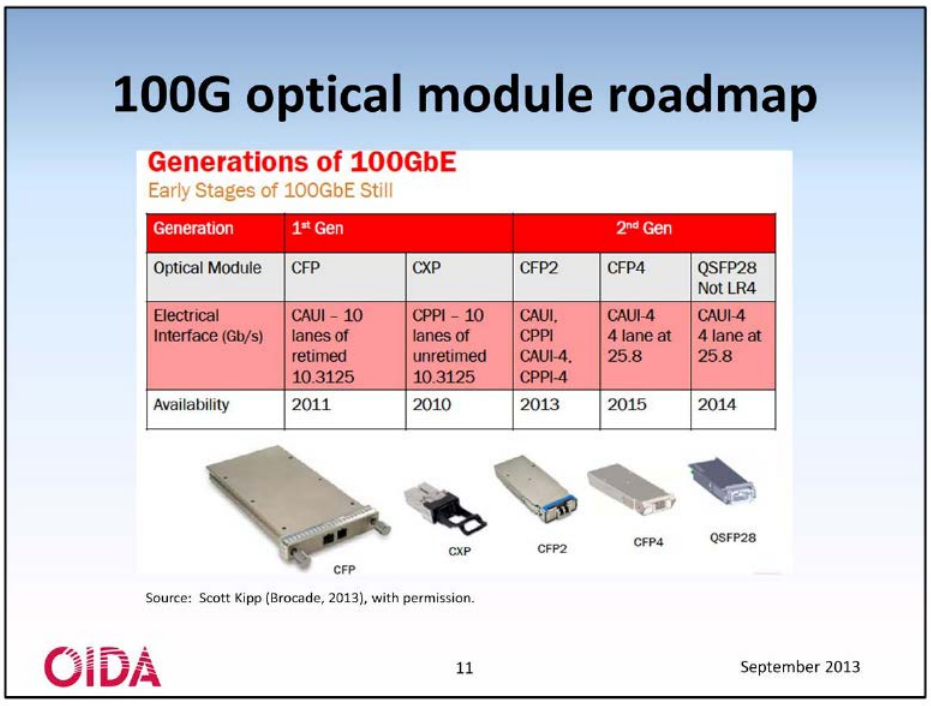
At the 2010 OIDA Annual Forum an analysis of local area network, metropolitan area network, and wide area network applications for photonic components was reported (see Figure 4).

A conclusion of this analysis is that network growth for consumer and business Internet use drives the need for faster and increased numbers of transmission ports in all network areas. In particular, the progression of optical modules used in Ethernet local area networks, both in form factor and in data rate, is driven by efforts to reduce package size while increasing data rate. (See reporting attributed to Scott Kipp of Brocade Corporation in the September 2013 *OIDA Market Update* and Figure 5.)




Source: R. E. Wagner (Corning Corporation), presentation at OIDA 19th Annual Forum, November 16, 2010.

**Figure 4. Network Applications for Photonics**




Source: OIDA, *OIDA Market Update*, September 2013.

**Figure 5. 100G Optical Module Roadmap**

The projection in Figure 5 shows that the current markets for optical technology initially start with components in large packages, and within a few years, with further development, they are optimized into a smaller form factor. This drive to smaller packages enables greater linear packing density (links per centimeter).

High bit-rate requirements for interconnects have emerged for data centers and high-performance computing applications (lower right corner in Figure 4). An emerging issue is the need to reduce the energy/bit as a means of reducing overall system power consumption. At a series of OIDA Workshops in 2011–2012,[3] which brought together representatives from the end-user data center resource management and the component supplier communities, projections of needed advances were discussed. The requirements for photonic interconnects resulting from these discussions resulted in the roadmap for technology development shown in Table 2.

**Table 2. Summary of Metrics for Data Center Networks**

| Metric | 2012 | 2017 | 2022 |
|---|---|---|---|
| Link speed (interconnect) | 10-100 Gbps | 100 Gbps to 1 Tbps | 250 Gbps to 2.5 Tbps |
| Cost per bandwidth (interconnect) | 1-5 $/Gbps | 0.50 $/Gbps | 0.025 to 0.15 $/Gbps |
| Energy per bit (rack-rack or greater) 1 pJ/bit = 1 mW/Gbps | 20-100 pJ/bit | 10-50 pJ/bit | 10-20 pJ/bit |
| Energy per bit (chip/board level link) 1 pJ/bit = 1 mW/Gbps | 2-10 pJ/bit | 1-5 pJ/bit | 1-2 pJ/bit |
| Optical switch port count Ref: CIAN | 200x200 | 400x400 | 1000x1000 |
| Optical switching speed (fiber & wavelength) Ref: CIAN | 10 msec (circuit reconfiguration) | 100 microsecond (per-connection reconfiguration) | 100 ps (packet-scale reconfiguration) |

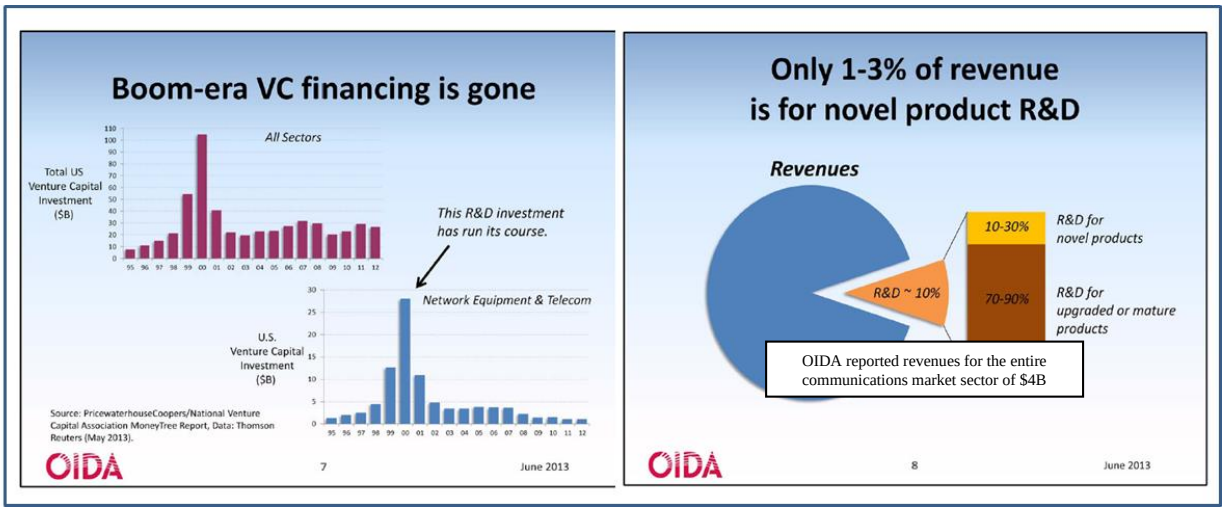
Source: OIDA Workshops on Metrics for Aggregation Networks and Data Centers 2011-2012, Final Report, April 2012.

This roadmap shows formidable technology challenges to be met, among them increasing interconnect speed by a factor of ~100, reducing switching speed by $10^5$, while also reducing the cost per bit transmitted by ~100.

Discussion at the OIDA workshops pointed out the importance of integrating photonic and electronic components to realize the roadmap goals. Finding the funding for the necessary research and development to advance the technology presents the difficult issue

[3] OIDA "OIDA Workshops on Metrics for Aggregation Networks and Data Centers, 2012," February 2012.

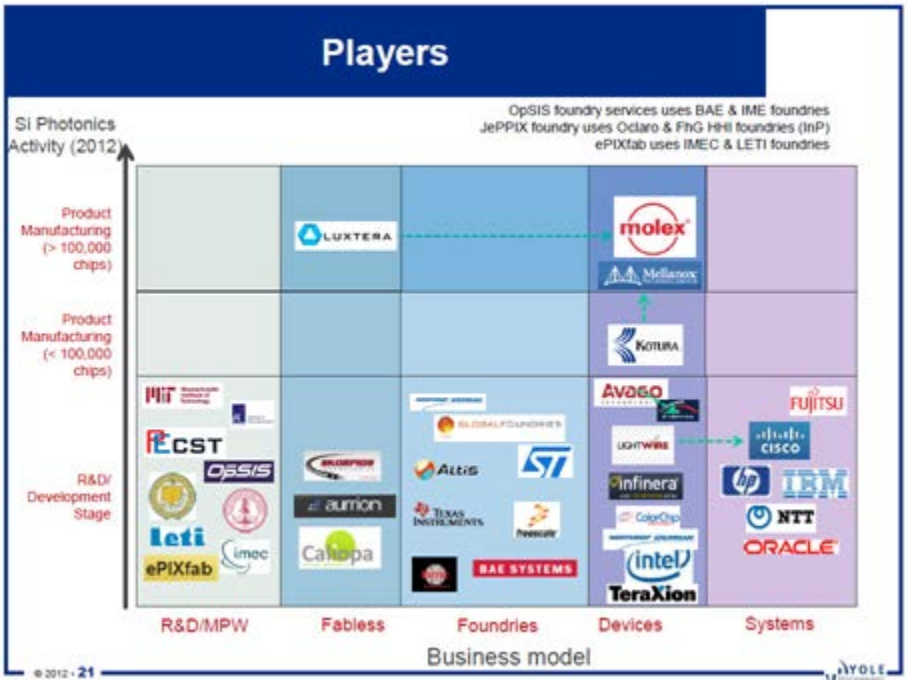
illustrated in Figure 6. Venture capital to support development of photonic technologies has been significantly reduced since the investor interest peaked more than a decade ago; at the same time the estimated 1–2% of revenues available for development of new products suggests a level of investment by industry for R&D on advanced components for communication applications of only about $40–80 million. This level of investment greatly limits opportunities for development of new and novel products. Some start-up organizations (e.g., Luxtera and Aurrion), presumably with venture capital support, have begun to develop and market silicon PICs to meet the goals cited in Table 2. Some major systems suppliers have also been willing to invest in on-going silicon PIC research and development efforts. Despite this, the attendees at the OIDA workshop judged it to be insufficient to support significant advancement by the companies themselves. It is noteworthy that comparable amounts are being invested by government agencies such as Defense Advanced Research Projects Agency (DARPA), National Science Foundation (NSF), Small Business Innovative Research (SBIR) participants, and others. The combined levels of R&D investment between industry and government suggest that there is some opportunity for both industry and government to leverage a PIC foundry ecosystem.




Source: *OIDA Market Update*, June 2013.

**Figure 6. Decline in R&D Funding**

Figure 7, published by Yole Développement, a European Union–based company that provides market research, technology analysis, and strategy consulting, gives a concise summary of the global silicon photonics development activity, showing the major companies and organizations involved in integrated photonics, along with their roles and business models. Note that since the compilation of this graphic, Kotura Inc. has been acquired by Mellanox Technologies Ltd., a networking company with headquarters in both Israel and the United States.



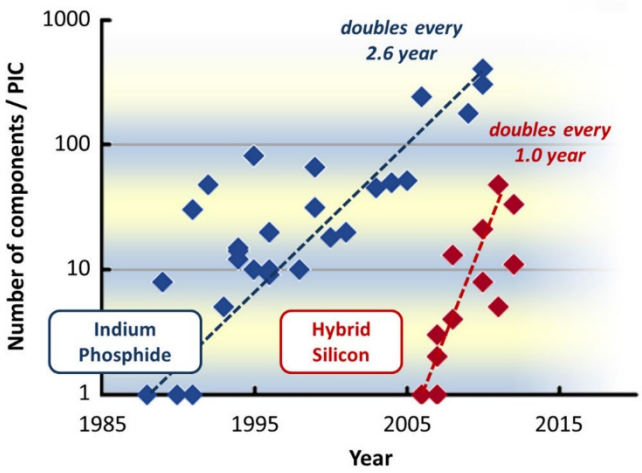

Source: Eric Mounier, "Silicon Photonics Market & Applications," LETI Innovation Days Conference, June 24, 2013, Grenoble, France.

**Figure 7. Silicon Photonics Development Activity**

## 3. Technology and Capability Analysis for Silicon PICs

### a. Silicon versus Indium Phosphide PICs

Both silicon and InP have been shown to have real promise for integrating photonics, especially when integration is also intended to include high levels of complex electronics. The InP materials platform is a compound semiconductor with inherent properties advantageous for photonics, such as the ability to make lasers. The silicon materials platform does not provide a monolithic laser in a practical sense, but the silicon/silicon-dioxide materials and its compatibility with other materials such as silicon-nitride and germanium do provide for a large range of photonics components. Although InP technology has demonstrated some remarkable successes (see the Infinera chip in Figure 3), InP fabrication facilities are not nearly as advanced or as widely available as those for silicon. Also, the flexibility available in the silicon-processing platform is expected to be of high interest in integrated photonics. Figure 8 illustrates how the level of complexity achieved using these two platforms has increased over the past decades.

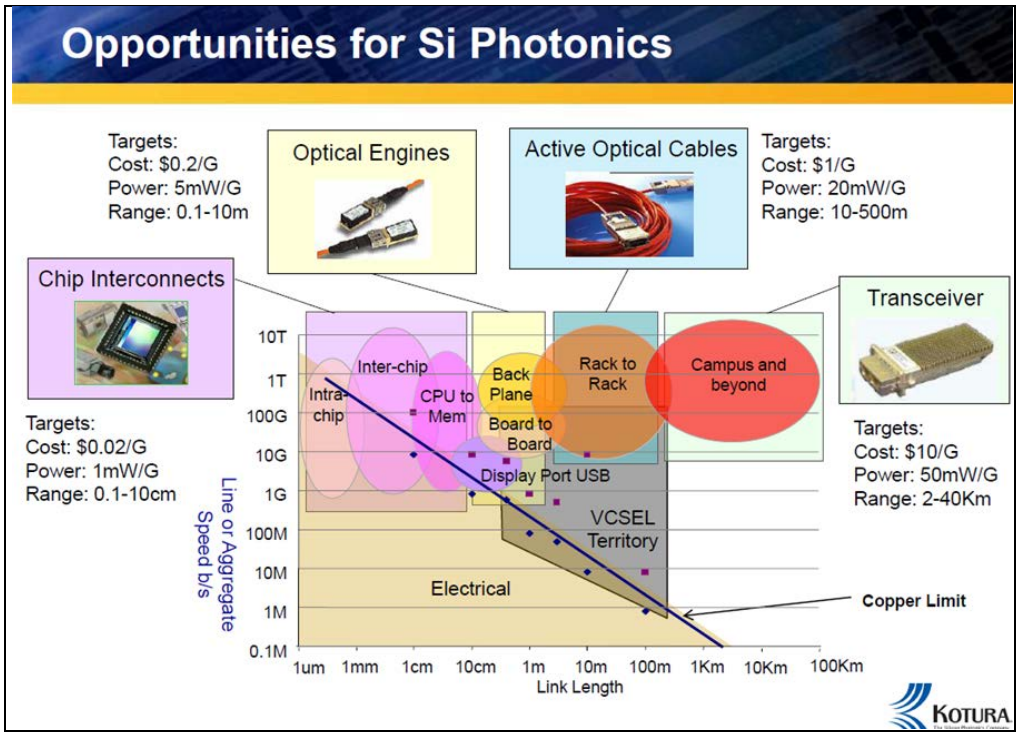



Source: M. J. R. Heck, M. L. Davenport, and J. E. Bowers, "Progress in Hybrid-Silicon Photonic Integrated Circuit Technology," SPIE Newsroom, doi: 10.1117/2.1201302.004730.

**Figure 8. Alternative Approaches to Achieving High-Density, High Performance PICs**

For InP PICs, the target market is currently telecommunications. Here, component cost has not been a primary issue for product differentiation, and there is a premium on designs that provide advanced capabilities for photonic signal processing (e.g., flexible light generation (multiwavelength) and detection (coherent)). On the other hand, silicon PICs typically target data centers and high-performance computing markets, where the relatively low cost, size, weight, and power achievable with a silicon platform are of primary concern. Figure 9 summarizes the key applications and markets for silicon PICs identified by Kotura (recently acquired by Mellanox) in the 2013 International Electronics Manufacturing Initiative (iNEMI).

For the purposes of this report, we focused on integrated silicon photonics as the technology platform for enabling innovations and new generations of integrated photonics components. At this time, we believe that the silicon-based fabrication technologies are the most likely to be widely available to researchers and small businesses, and they can be easily adapted to accommodate most of the applications. Although the recommendations may well be extended to an InP PIC foundry and there are some technological advantages to InP as a substrate, the primary target is silicon photonics. In the remainder of this report, references to "photonics foundry" are to a silicon photonics foundry.




Source: iNEMI, *2013 Roadmap*.

**Figure 9. Opportunities for Silicon Photonics**

### b. Silicon PICs in the Context of the Evolution of the Silicon Business

The semiconductor IC business has evolved to embrace multiple engagement models. In comparison, integrated photonics technology is in its infancy. This study assumed that the emerging photonics business could leverage the successful models established in the silicon IC market. For silicon ICs, four major product-development models have been successful: integrated device manufacturer (IDM), collaborative development, application-specific integrated circuit (ASIC) model, and foundry model. These are examined as the basis for alternative models for a silicon PIC business. Companies may offer products and services that span more than one model. Note that some of the silicon IC models have grown in an evolutionary manner in response to larger market forces and global competition; the silicon photonics market is also expected to be shaped by similar forces. Each model is discussed in turn.

#### 1) Integrated Device Manufacturer

A single company develops products and manufactures them, often using proprietary processes and knowledge. Often these companies, like Intel in electronics or Infinera in InP photonics, achieve high performance by tightly coupling the entire product-development and manufacturing process. In electronics, this model has been

most successfully used by companies that have established a unique product family and generally follow a technology roadmap articulated in the International Technology Roadmap for Semiconductors. The IDM model is not directly appropriate for an open accessible foundry for integrated photonics because the typical IDM company takes significant advantage of a tight optimization of design into the special features of the manufacturing capabilities.

**2) Collaborative Development**

A project development by a flexible, proprietary, and strategic collaboration between a product developer and a manufacturer. Often these arrangements are individualized and can involve high levels of cost and commitment between the players. The success of these endeavors usually involves shared risk between the product developer and the manufacturer. IBM is an example in this category. IBM has announced a foundry flow for certain types of integrated photonics devices, and it is looking for external application partners to complete its technology development, although IBM does not produce these components as an original equipment manufacturer. In a collaborative development, ownership of intellectual property (IP) and rights to its use are usually negotiable.

**3) ASIC Model**

A product developer provides the manufacturer with a specific, formal description of the product, and the manufacturer agrees to perform the detailed physical design for the specified product and to manufacture it. This model has the manufacturer taking on most of the risk. In photonics, Luxtera follows this model, offering its design team and expertise in fabrication to other companies, such as Oracle. In such cases, Luxtera arranges for the production of components, engaging with a third party that takes on the full responsibility for the project. Luxtera does not have its own semiconductor processing facility, but relies on collaboration and contract manufacturing by others such as Freescale and ST Microelectronics N.V. (ST) in France.

**4) Foundry Model**

A product developer takes on the responsibility of performing a physical design of the product and passes what are essentially manufacturing instructions (through process selection and mask data) to the manufacturer. The manufacturer ensures that the described product is manufactured as specified, but the product developer is ultimately responsible for whether the product design is successful. A foundry does not usually compete with its customers by developing similar products under its own name, and foundries follow strict rules to protect customer IP assets. More formally, we consider a foundry to be a manufacturing capability with the flexibility to produce different configurations of design elements to create different products serving different customers

and different markets. Its underlying processes are stable and reproducible independently of any particular configuration that may be currently in production. Foundries range from being completely open, accepting designs from virtually anyone, to being more selective. The Institute of Microelectronics (IME) in Singapore, Laboratoire d'électronique des technologies de l'information (LETI) in France, Imec in Belgium, and Sandia National Laboratories in the United States are examples of organizations that have offered foundry-type access to silicon processes for integrated photonics.

We refer to these four basic models in our examination of alternative models for a photonics foundry (see Section D).

### c. How the Foundry Model Works

Figure 10 summarizes the typical flow employing a foundry fabrication service that takes a new product or research concept to produce samples. Such services are typically funded by the government (DARPA, NSF, SBIR, etc.), by internal means (Independent Research and Development, Laboratory Directed Research and Development, etc.), or by an investor to produce samples that can be the basis for research publications or product prototypes that, in turn, can attract further investment leading to a commercial product.

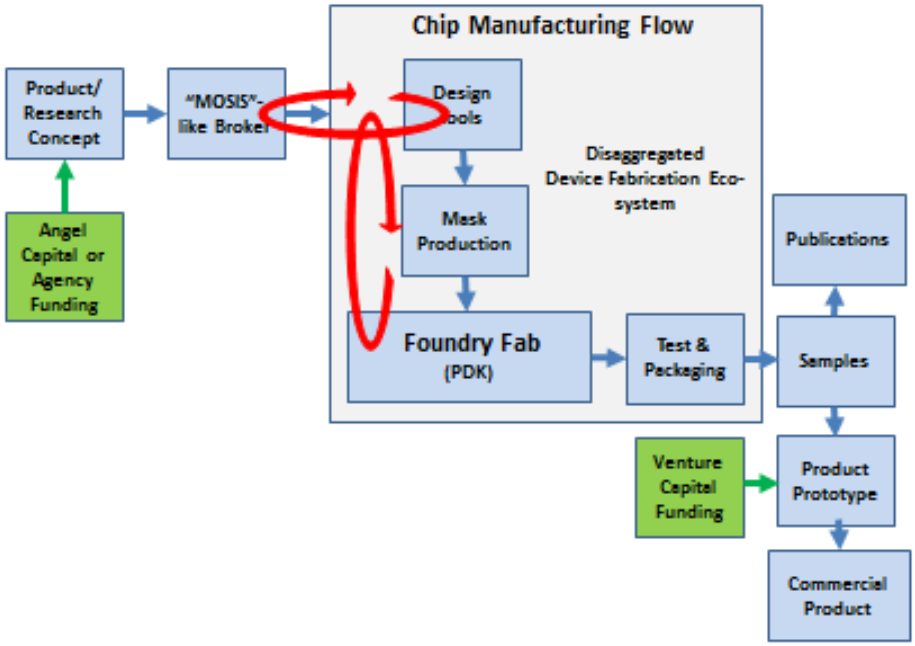



**Figure 10. Foundry Flow**

An explanation of the foundry ecosystem illustrated in the figure follows:

- An academic researcher or industry foundry customer creates a project to prototype a new photonic component and seeks either government, industrial, foundational, or

angel funding to develop this prototype as the basis for research publications or to attract further investment leading to a commercial product.

- This customer develops a high-level design that is often simply described in terms of interconnected components or "blocks." Computer-aided design (CAD) tools optimize and translate these interconnected blocks into the masks that define the various layers and manufacturing processing steps to produce the finished chips.
- These processes are specified by the foundry fabrication service in what is referred to as a process design kit (PDK). PDKs can be complex, essentially containing the process information used to process starting silicon wafers into finished components. PDKs can also contain devices and structures, but are usually developed by, and unique to, the fabricator.
- The tools employed from concept to finished sample chips include the foundry PDK and also test and packaging. Test and packaging functions ensure that the processing of the wafer has been successful (e.g., the measurements on separate test structures are incorporated into the masks used to fabricate the components to determine if any flaws occurred during process), packaging includes dicing the wafer into chips and mounting them on a chip carrier substrate for packaging and delivery to the customer for functional testing of whether the chip performs as planned.
- The microelectronics industry has evolved to the point where the supply chain is so fragmented that many of the tools employed from concept to finished sample chips, including test and packaging, have been developed by separate organizations, and an independent broker function has emerged to assist the uninitiated researcher or product developer in interfacing to these resources.
- With detailed knowledge of the manufacturing flow (PDK), the broker can play an important role, efficiently working with multiple customers. The red arrows in Figure 10 reflect the iterations in the design process. These iterations are often required to achieve a satisfactory design for fabrication using CAD tools that the customer either licenses from the foundry or broker or develops independently. Typically, the broker checks design rules and manufacturability of the customer-specified component design, generates final layout and transmission of design to the foundry, schedules and coordinates the submission to the fab, and aggregates different designs into a single layout for multiproject wafer (MPW) fabrication (multiple designs typically from different customers processed on a single wafer).
- The foundry normally is responsible for mask fabrication, processing the wafers, and wafer-level testing.

- Typically, the foundry provides the fully processed wafer to the broker who then is responsible for oversight of wafer dicing into chips and initial packaging and distribution of unpackaged die, or packaging on a chip carrier.
- The customer or test house is responsible for functional testing and obtaining any final packaging of the chips.

## 4. Key Blocks

Table 3 provides overview of the generic integration manufacturing services and building blocks available at some selected foundries. Note that this information is somewhat dated (October 2012).[4] Appendix D provides more detailed descriptions of these component building blocks.

**Table 3. PIC Building Blocks**

| Foundry | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| Technology | SOI | SOI | SOI | SOI | SOI | InP | InP | InP | $Si_3N_4$ | $Si_3N_4$ |
| Open access | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | ✓ | ✓ |
| Access mode | MPW | MPW | Dedicated | MPW | MPW | MPW | MPW | MPW | MPW | Dedicated |
| Cost per | Area | Area | Project | Project | Area | Area | Area | Area | Area | Project |
| Packaging | ✓ | | | | | ✓ | ✓ | | | |
| Photonic Design Kit (PDK) | ✓ | | | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | |
| Electronics | | | | | ✓ | | | | | |
| BUILDING BLOCKS | | | | | | | | | | |
| Shallow Waveguide | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| Deeply Etched Waveguide | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ |
| Waveguide crossing | | | | ✓ | | ✓ | ✓ | | ✓ | |
| Y-Branch | ✓ | ✓ | | ✓ | ✓ | ✓ | | | ✓ | ✓ |
| Directional Coupler | ✓ | ✓ | | ✓ | ✓ | | | | | ✓ |
| Multimode Interference Coupler | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | | ✓ |
| Single Polarization Grating Coupler | ✓ | ✓ | ✓ | ✓ | ✓ | | | | | |
| Polarization Splitting Grating Coupler | ✓ | | | ✓ | ✓ | | | | ✓ | |
| Spot-Size Converter | ✓ | | | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ |
| Electro-Optical Modulator | | | | | | | ✓ | ✓ | ✓ | |
| Thermo-Optic Modulator | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | | |
| Carrier-Injection Modulator | ✓ | ✓ | | ✓ | | | | | ✓ | |
| Ring Resonator | ✓ | ✓ | | ✓ | | | | | | |
| Arrayed Waveguide Grating | ✓ | | | ✓ | | | ✓ | ✓ | | |
| Distributed Bragg Reflector | | | | ✓ | | | ✓ | | | |
| Semiconductor Optical Amplifier | | | | | | | ✓ | ✓ | | |
| Photodiode | ✓ | ✓ | | ✓ | ✓ | ✓ | ✓ | | | |
| Balanced Photodiode | | | | | | ✓ | | | | |

✓ *Generic bulding block available*

Source: Pascual Muñoz, *Towards Fabless Photonic Integration*, VLC Photonics White Paper, October 2012.

## 5. Electronic Design Automation

To realize silicon PIC for various photonics components, such as waveguides, grating couplers, modulators, germanium-on-silicon detectors, and passive devices, U.S.

[4] The technologies include silicon photonics represented by silicon on insulator and silicon nitride ($Si_3N_4$) as well as the as III-V material InP. (III-V materials are elements from groups III and V of the periodic table.)

industry is slowly developing the tools to support a design software ecosystem. Fabricators that are following the IDM model usually also have in-house capabilities to perform designs, and those tools could be adapted to provide foundry access, but a true PIC foundry-centered design environment analogous to that in microelectronics does not exist yet. The design ecosystem starts with guidelines for an early design kit using available design libraries and a loose collection of CAD tools for integrated physical, circuit modeling and simulation, layout, and schematic verification. The capability for integration of design tools mostly exists in a few companies that have co-developed proprietary tools and services that take advantage of open interfaces that the major electronic design automation (EDA) vendors—Cadence, Mentor Graphics, and Synopsis—provide to their design systems.

The PIC CAD industry is still in its infancy because of low volume and cost considerations. Mentor Graphics, teaming with OpSIS (http//opsisfoundry.org) and foundries (IME Singapore), has demonstrated a prototype full design implementation and verification flow for the IME Silicon Photonic process. The flow uses the Mentor Pyxis Custom IC Design Platform for schematic capture and schematic-driven layout, along with the Mentor Calibre nmDRC and Calibre nmLVS tools, with detailed parameter checking for physical verification of the design. Figure 11 shows the major software components in the Mentor Graphics IC design environment and design kits.


Source: Mentor Graphics, "Mentor Graphics Teams with OpSIS Foundries and Lumerical Solutions on PDK Development for IME Silicon Photonics Process," Mentor Graphics News Release, May 22, 2013.

**Figure 11. Mentor Pyxis Schematic**

Luxtera, another fab-less silicon photonics company, has partnered with EDA vendor Cadence and the Freescale silicon IC foundry (and ST Microelectronics more recently) to develop their own proprietray design tools for photonic device integration.

That environment integrates the Luxtera PDK and prorietary design tool environment with a component library (optics and electronics), simulation platform (models/corners and process parameters), and physical verification tools (DRC, LVS, etc.) for IC integration.[5] Discussions with Aurrion and other companies working in the field reveal similar approaches.

### 6. Important Lessons: MOSIS Foundry Success Story

The Metal Oxide Semiconductor Implementation Service (MOSIS) was established to provide researchers with fast, low-cost implementation of research chips in silicon. Originally funded by DARPA and the NSF, MOSIS provided a broad range of services and access for the research community.[6] These included design methodologies, tools, IP, and cost-effective access to foundries. A key element of providing cost-effective access was the use of MPW, which enabled nonrecurring costs for production runs over multiple projects to be shared. Additional MPW cost savings were obtained by leveraging ongoing relationships between MOSIS and the foundries, spreading or avoiding access fees, and avoiding inefficiencies that result when high-volume foundries serve low-volume customers.

MOSIS hosted an education program that gave researchers discounted or free access to foundry services. In 1998, direct government funding for MOSIS ended after 15 years of support, and the program became self-sustaining. Today, MOSIS continues to provide cost-effective access to foundries through its MPW program. It also operates the MOSIS Educational Program, which provides support for unfunded research conducted by graduate students and faculty from certain universities. The MOSIS Educational Program provides limited access to two fabrication technologies (0.5 micron and 0.18 micron CMOS) that are considered as trailing-edge for microelectronics purposes.

## C. Proposed Target PIC Foundry: Gap Analysis

As mentioned before, the goal is to establish an academic-industry-government collaborative center in the United States to advance the research, development, manufacture, and assembly of complex integrated photonic-electronic devices. To achieve that goal, we examined the ecosystem that is needed and identify any gaps. The elements of the ecosystem have five components:

- Foundry (wafer fabrication)
- Design tools (design automation)
- Intellectual property

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[5] Luxtera, “LuxG Process Specifications,” 2011.

[6] The MOSIS Service website, “A Brief History.”

- Packaging
- Testing

In Section D, we examine how each of the alternative models can provide these key elements of the ecosystem.

Although many gaps in providing seamless access to PIC foundry services currently exist, use of the foundry ecosystem is expected to close most of these gaps. That is, as users drive demand, the gaps will be closed naturally, suggesting that there is no need to invest heavily in closing any single gap at present.

### 1. Foundry (Wafer Fabrication)

Silicon-on-insulator (SOI) wafers, used as starting material for many silicon photonic applications, are a standard product of many high-volume silicon IC manufacturing fabrications. SOI wafers are both compatible with the silicon fabrication environment and are readily available from commercial sources in the requisite sizes and parameters (layer thicknesses, flatness, etc.). Current silicon fabrication lines can use SOI wafers without any concerns. One of the leading suppliers of SOI wafers is Soitec, headquartered in Bernin, France.

A number of domestic sources in the United States could potentially supply foundry capacity for silicon photonics. Luxtera, a fabless U.S. company, has developed and is marketing silicon photonic products employing U.S.-based fabricators. It has developed proprietary recipes for a number of photonic devices. OpSIS, based at the University of Delaware, operates a MOSIS-like MPW service for silicon photonics devices relying on Singapore's Institute of Microelectronics foundry services. OpSIS, which has developed a limited number of tools to help engineers design and simulate silicon photonic devices, represents an established resource with several years of experience providing MPW silicon photonic services.

InP wafers are brittle relative to silicon and are not compatible with existing silicon fabrication facilities in terms of form factor[7] and potential contamination to the tooling. The brittleness of the InP wafer makes it more challenging for automated wafer-handling systems, which can limit the practicality of larger diameter wafers. The primary supplier of high-quality bulk and epitaxial InP wafers is IQE, headquartered in Cardiff, Wales.

At the present, there is little InP fabrication capacity in the United States besides high-speed electronics and photonic devices for telecommunications. These companies

[7] Wafers of 3 to 4 inches are typical for InP electronics, and 6 inch wafers are available; silicon processing is typically done with 200 mm and 300 mm wafers, less so with 150 mm wafers).

that fabricate components in the U.S., like Infinera, are operating as IDMs and consider their expertise and processes a competitive edge. The risk of compromising their competitive advantage by taking on InP fabrication is simply too high. As a result, little InP foundry capability is expected in the United States.

### 2. Design Tools—Electronic Design Automation

The three major EDA companies, Cadence, Mentor Graphics, and Synopsis, have only recently started to venture into the photonics market. Their approach has been growth through acquisition; they acquire small companies that offer specific photonic design expertise and integrate the acquired companies' products into their design platforms (e.g., recent Synopsis purchase of RSoft). This path is typical for EDA companies seeking to expand into the photonics market.

The capability gap at the design stage is still significant. Electronic design software has a greater level of maturity and abstraction than that for photonic design. For example, a digital IC designer does not need to account for all the underlying device physics of the transistors in the circuit. The tools have become sophisticated, allowing designers to work with higher level abstractions and manipulate functional blocks. EDA software takes care of the underlying physics and identifies any suspected electronic issues (cross-talk, timing, power dissipation, etc.), freeing the designer to become more productive and create innovative functionality. Electronic circuit designers have numerous tools to verify, validate, and simulate their work. For foundry flows, the EDA vendors develop suites of tools to be compatible with the specific PDKs from each fab as well as programs for checking design rules. The interface is virtually seamless.

Photonics design tools for foundry support, on the other hand, are at roughly the maturity level that IC design tools were about 30 years ago. The photonics designer still needs a significant amount of knowledge of the underlying optics, materials science, and physics to ensure that the design will work as intended. Several necessary CAD tool modules do not exist or are very primitive (e.g., verified photonics IP blocks, high-level design, verification). This prevents foundry-sourced integrated photonics from achieving a state analogous to foundry-sourced microelectronics today. The coupling between the fabricators and the design tool developers is still rather weak. Today, anyone working on product development of integrated photonics uses a mix of in-house and commercial tools to accomplish a design, but the fabrication facilities are not operating as pure foundries. The basic CAD capabilities largely exist to accomplish a physical design, but efforts are needed to fully support an open foundry concept for fabrication.

### 3. Intellectual Property Protection

The significant cost of designing a state-of-the-art semiconductor IC is a major portion of the nonrecurring expenses in the development of new products. Therefore, to

keep costs manageable, many designers re-use proven functional blocks, commonly known as semiconductor intellectual property, called semiconductor IP.[8] A major market has developed in semiconductor IP, with companies like ARM generating significant income from licensing IP. By using semiconductor IP, IC designers save considerable design time (and therefore money) by getting a design proven in silicon, and they know exactly how it will work. The term for companies that only provide semiconductor IP is "chipless."

Photonics has not yet reached the level of maturity and standardization to support a market in photonic IP. This is a significant gap, which if addressed, can accelerate the adoption of photonics technology. We are aware of development work and technical announcements by multiple researchers on IP related to individual components.

## 4. Packaging

Photonic packaging is often the most expensive part of a photonic circuit. Not only do many photonic circuits require reliable electrical interfaces, they often need interfaces with external optical signals and external optical fibers. The large mismatch between the diameter of the most commonly used single-mode fibers and the size of a typical waveguide on a photonic IC presents severe alignment and signal-attenuation challenges. Successful packages have been developed that solve these problems for areas like telecommunications, but they are relatively expensive. Furthermore, not only does the die itself have to be hermetically sealed in a protective environment, the package must maintain the alignment between the incoming and outgoing optical fibers and the photonic integrated circuit through many thermal and mechanical cycles.

In a limited number of cases, such as the camera sensor in a cellular phone or a vertical-cavity surface-emitting laser (VCSEL) in an optical computer mouse, inexpensive packages suitable for high-volume consumer electronics markets have evolved. These cases, while exceptions, demonstrate that with a sufficient market and demand, engineers can solve the problem of packaging cost and complexity and develop economical solutions.

The analogy of a 30-year lag of photonic IC technology maturity relative to the semiconductor IC maturity also applies to packaging. Frequently, TO-5 and TO-33 packages with optical windows house photonic devices. The semiconductor industry developed this type of packaging to house individual transistors about 40 years ago. This type of packaging is not likely to be applicable to future photonic ICs that need more sophisticated electrical and optical interfaces to the rest of the system to be useful.

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[8] In this context, semiconductor IP is not the same as intellectual property as commonly understood.

## 5. Testing

Semiconductor IC fabrication relies on early detection of defective devices to minimize the number of components that will not function as designed. In-process and on-wafer semiconductor testing has become a highly sophisticated process. Semiconductor equipment manufacturers have developed special high-speed tools like the CD-SEM to measure critical dimensions. IC fabricators put special test structures in the kerf areas between individual dies on a wafer. During processing, the fabricators can probe these special structures and measure critical dimensions to determine if the process steps to that point will result in devices whose performance will fall within specification limits. If a sufficient number of tests indicate that the wafer will likely not yield an economic number of functioning dies, the wafer can be pulled from the line. In this manner, the fabrication minimizes the amount of value it invests in a wafer that will yield no revenue.

Similarly, before a wafer is diced and the individual chips packaged, every die on the wafer often is probed and tested. Defective dies are marked and discarded, saving packaging costs. In many cases, packaged dies are placed in a special oven for a process known as “burn in,” where the dies are stressed to find early failures and thereby eliminate a marginal fraction of the total population.

There are few tools and infrastructure for testing complex photonic circuits on a wafer. Photonic device testing is complicated because both optical and electrical parameters are usually important, and it is difficult to extract light from, a die that has not been separated into individual die and packaged. Without adequate ways to test a die before packaging, a defective die results in a discarded package—often the most expensive part of the whole photonic product.

This lack of test and measurement equipment and techniques provides an immense economic barrier to the growth of the photonic IC market. Although the total market is not yet large enough to drive the emergence of this infrastructure itself, with sufficient growth in the photonics market, it can be expected that investments naturally will be made to address this gap.

## 6. Education

Complete fabrication facilities in an academic environment have become too expensive and impractical to build and maintain. Fabrication facilities require a highly controlled and stable set of processes and a dedicated team of engineers and technicians; the academic environment is not conducive to this level of control, and the volumes associated with economical processing make it impractical for every research organization or university to practice. Many of these same researchers are able to get circuits fabricated through their relationships with the companies and organizations that do operate fabrication facilities.

Since its establishment about 40 years ago, MOSIS has served as an interface for researchers and prototype designer to the foundries in state-of-the-art semiconductor facilities. MOSIS organizes and manages multi-project wafer fabrication runs for multiple foundries, allowing individual designers to submit their designs to MOSIS where they are aggregated into a single design submission to the foundry. This aggregation allows for efficient use of resources, including not only the semiconductor area but also the engineering effort, since MOSIS can serve as the foundry's agent for handling technical issues.

Over the years MOSIS has shifted its role from mainly supporting academia to also supporting industry, especially for prototyping and low-volume access to state-of-the-art semiconductor manufacturing. The United States has no comparable experience base with aggregation for photonic fabrication in a foundry. The Canadian Photonics Fabrication Centre, established in 2012 by the Canadian Government, may be a good model for any similar efforts in the United States.

## 7. Alternative Models

This report considers four alternative models for establishing a photonics infrastructure:

- Integrated device manufacturer
- Collaborative development
- ASIC model
- Foundry model

For researchers and small business innovators, the key attributes this ecosystem needs to attain are having access to advanced technology, being affordable at low volume, providing easy transition from low/prototyping volumes to high volume, and offering sharing and leveraging of pre-competitive resources while enabling innovation.

Table 4 evaluates each model against these four attributes. The IDM and collaborative development models are ill suited to support low-volume research and small industry efforts. They are expensive and have difficulties working with academia. The ASIC model is a potential candidate that would be more affordable and amenable to engaging with low-volume customers. But the ASIC model is still expensive because the fabrication cost will not be shared over many projects as can be achieved with MPWs in the foundry model, and the ASIC model does not directly support component-level innovations that researchers might want to pursue. Therefore, we conclude that the foundry model, based on a silicon photonics platform, is the most promising candidate.

**Table 4. Alternative Model Stoplight Chart**

| Alternative model | Advanced technology access | Affordable | Easy transition to production and marketing | Sharing and leveraging of innovation |
|---|---|---|---|---|
| Integrated device manufacturer | Advanced | Expensive | Hard | Hard |
| Collaborative development | Advanced | Expensive | Medium | Hard |
| ASIC model | Modest | Modest | Easy | Modest |
| Foundry model | Advanced | Affordable | Easy | Easy |

## D. Roadmap

Here, we suggest the first steps to address the key gaps and estimate the resources needed. The assumptions here are that a suitable semiconductor-fabrication facility is the focal point for the physical processing and that semiconductor facility already has an optical process in place. Funding for the complete development of a new process or making substantial enhancements is not envisioned within this roadmap. In Appendix B, we examine some conditions to suggest a threshold in terms of numbers of runs and costs needed to establish a viable foundry ecosystem. This assessment suggests that three to four MPW runs per year are needed to keep the ecosystem viable.

### 1. Broker Development and Foundry Qualification

We recommend making the existing silicon fabrication infrastructure available to the photonics development community and avoid developing new facilities. New process design kits will need to be developed and calibrated. Tools that support design rule checking and other methods for connecting the development community to the manufacturing environment will be required. The photonics fabrication process will need to be qualified to ensure that the design kits are true representatives of their physical instantiation in silicon. Furthermore, processes and tools for aggregating and merging design for MPW runs will need to be in place. We recommend leveraging existing organizations to the greatest extent possible. Based on knowledge of costs associated with comparable services, the team developed some rough estimates of the level of resources needed for broker development and foundry qualification.

### 2. Enterprise Discount Program

A program that supports discounted access for qualified academic or industrial research programs, as well as for government use, will encourage utilization early on and build momentum in the use of the photonic foundry ecosystem. It is suggested that funds for the discount program could be designated from the start to phase out within 2–5 years as soon as utilization of the foundry ecosystem becomes self-sustaining. More funding could be designated to reach more researchers or encourage multiple design efforts within

a research group or more frequent runs. Various criteria could be developed for applying the discounted access, such as first-come first-served, cost-matching to outside funds, and alignment to agency priorities.

### 3. Photonics Education Program

A research program modeled on the MOSIS Education Program would totally or partially subsidize the cost of foundry services for selected students (for coursework prototypes) and researchers (primarily academic). This program would fund innovative ideas and concepts for PICs that would be fabricated via the foundry technology. A quick survey sampled photonic prototypes and identified that typical researchers used about 32 $mm^2$ for their design. The foundry cost of services currently provided by organizations like OpSIS is about $2,000 per $mm^2$ for a MPW run,[9] which delivers 20 bare dies. This suggests that the fabrication costs for each project is likely to be about $64,000. This cost does not include additional costs related to design, packaging, or testing. We suggest that this program be an ongoing initiative.

### 4. Photonics Packaging and Test

A successful ecosystem will need cost-effective packages that support a wide range of photonic devices and the ability to test those devices during fabrication. Such testing will require significant investment. As packages, test equipment, and processes are developed, benefits will flow so that high-volume consumer markets develop. In the interim, a modest effort focused on developing basic capabilities and standards is appropriate. This area will require close monitoring and likely an infusion of significant additional funds. At this stage, it is too early to predict the appropriate path.

### 5. Photonics Fabrication Training

Course materials on the methodologies, tools, and techniques for using the photonic foundry will be required. We suggest making a concerted early effort to develop and deploy these materials. The eventual broker will likely be the most suitable conduit to distribute them to the academic community. We recommend leveraging the experience and existing base of OpSIS for more efficiency. We further recommend that this effort take advantage of the lessons learned by the Canadian Photonics Fabrication Centre in its experience with the academic community. The educational aspect will likely require ongoing support for a decade.

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[9] OpSIS website, “Standard Pricing for MPW Schedules,” OpSIS IME-004 and IME-005.

## E. Conclusions

Existing domestic photonic foundry capabilities are sufficient to support a wide range of research into innovative photonic components and applications. Key gaps exist in design tools, IP, packaging, testing, education materials, and funding for researchers in terms of appropriate discounts and sources of support for unfunded academic researchers.

To facilitate making these capabilities available in a cost-effective manner to researchers and small industrial efforts, we recommend that an ecosystem be established with initial government support. A key component of this is a broker to (1) act as an intermediary between users and fabricators; (2) orchestrate the design, fabrication, packaging, and testing; and (3) develop MPW capabilities to reduce individual user costs. Maintaining this ecosystem can be expected to help close the gaps in wafer fabrication, EDA, IP protection, packaging, and testing.

It is likely that an implemented program would undertake some parallel efforts to reduce risk and select additional technologies for broader access, which might require a higher level of funding. A successful photonic foundry program can be expected to transition towards being substantially self-sustained within 5 years by having users pay for their services. If possible, a separate effort to fund photonics R&D that uses the foundry ecosystem could accelerate both the development of a strong user community and progress towards self-sustainment. A complementary R&D effort would make substantial progress towards those goals.

# Appendix A.
# Silicon Photonics Market

Silicon photonics technology often involves a range of integrated heterogeneous technologies mixing optics, CMOS, MEMS, and three-dimensional stacking technologies. All these technologies converge in silicon photonics.

At a photonic system level, a 2008 estimate of the total world industrial market for civil and defense photonics was approximately $440 billion.[1] The two largest civil sectors were flat-panel displays and information technology, which accounted for $97 billion and $67 billion, respectively. Together, these two sectors made up nearly half the total market volume (44%). The overall production of defense-related photonics end products in 2008 was estimated by the same source to be $30 billion, a substantial portion of worldwide defense procurement. By comparison, in 2009, European production reached $60 billion and U.S. production $154 billion in 2009 (EDA).[2]

At a photonics component level, a more recent OIDA market survey[3] estimated total U.S. photonics components production in 2012 to be $24 billion. Key market segments include solar ($6 billion), sensor and imaging ($4.8 billion), communications ($4 billion), optics ($3.3 billion), industrial and laser ($2.8 billion), cooled fiber ($1.9 billion), and LEDs ($1.6 billion). The photonics market is in its infancy but gaining ground as a low-cost alternative technology that can address speed and bulk data transfer challenges faced by microelectronics.

According to Yole Développement,[4] the silicon photonics market primarily operates in low volume in terms of dies and wafers, with an estimated 500,000 chips shipped over the last 5 years, which represents a few thousand 200 mm wafers. As shown in Figure A-1, silicon photonics sales are poised to quadruple over from ~$55 million in 2010 to ~$215 million in 2017. In 2017, silicon photonics products are forecast to make up 2% of the total $9.5 billion optical components industry.

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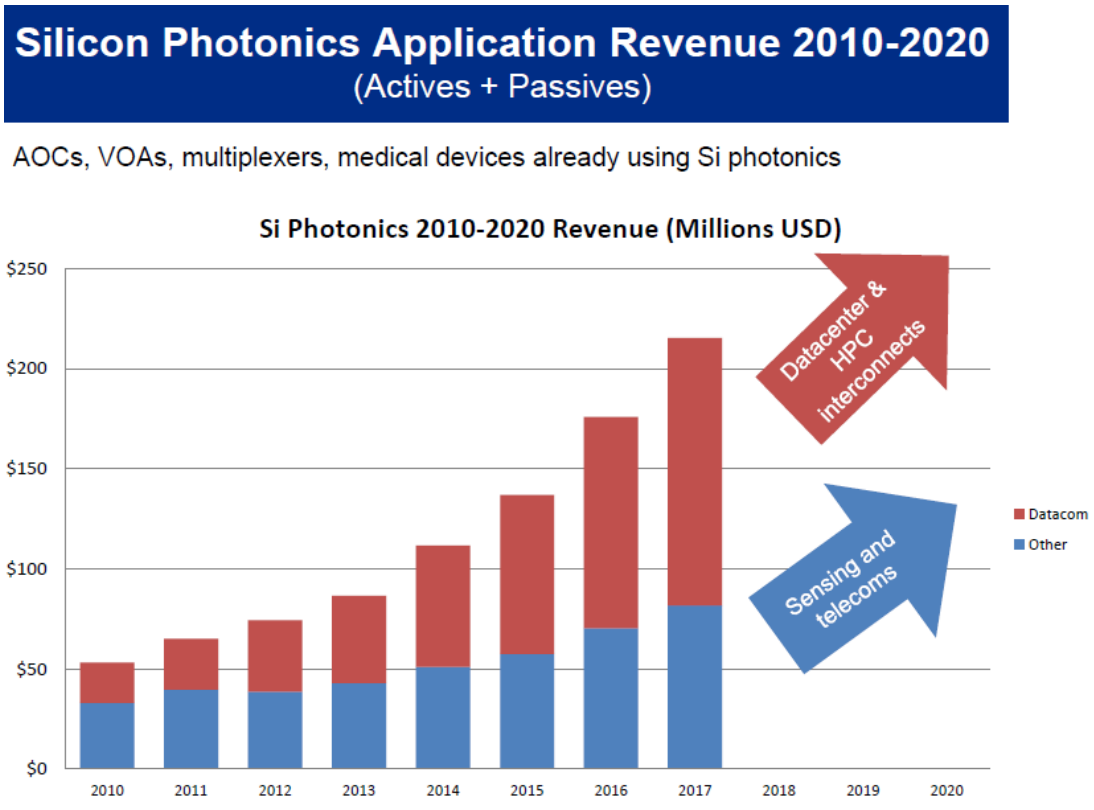
1 Optech Consulting, April 2010.

2 M. Butter et al., *The Leverage Effect of Photonics Technologies: The European Perspective*, Photonics21 (European Commission, March 2011).

3 OIDA, *Market Update*, May/June 2013.

4 Yole Développement, "Silicon Photonics Market & Applications," EPIC 2012, July 2012.




Source: Yole Développement, "Silicon Photonics Market & Applications," EPIC 2012, July 2012.

**Figure A-1. Silicon Photonics Application Revenues**

Data communications is the market that will dwarf all other silicon photonics applications. Major communication protocols are all moving to high-speed signaling and at rates of 10 Gbps, where reach and signal-integrity issues are surfacing for both copper and optical technologies. The clear trend is to surpass 25 Gbps in communication rates, which is where silicon photonics will have an advantage. The need will be driven by low-cost, high-speed interconnects supporting ever-increasing data rates at and beyond 25 Gbps, and the limitations of VCSELs, which have trouble reaching past 70 meters at 25 Gbps and above.

Among all the silicon photonics products, the wavelength division multiplex filters contributed $35.2 million to the global silicon photonics market in 2010. Most of this figure is due to early commercialization of these filters and their extensive usage in optical switches and transceivers devices. The silicon photonics light-emitting diode market is expected to grow at a relatively high compound annual growth rate (CAGR) of 87.6% from 2010 to 2015, due to an increasing need for efficient light sources in small distance communication networks. At present, Northern America dominates the silicon photonics market, generating $59.6 million in 2010, and it is expected to reach $850 million in 2015 with a CAGR of 70.1% from 2010 to 2015.

The silicon photonics market is expected to be commercialized by 2016. Today, few companies are actually shipping products to the open market. Some of the major players in the global silicon photonics market are the U.S. firms Kotura, Lightwire, Luxtera, and Chiral Photonics.[5]

Another forecast expects the photonic component market to grow from $150.4 million in 2012 to $1,547.6 million by 2022, at an estimated CAGR of 26.3% from 2012 to 2022.[6] The major players in the PICs industry are Infinera Corporation, NeoPhotonics Corporation, Oclaro, Luxtera, Kotura, and OneChip Photonics. Among the innovations, Infinera has introduced 500 Gbps PICs used in long-haul flex coherent super channels. The main features of these products are simplicity, scalability, efficiency, and reliability. And Neophotonics has developed an optical line terminal transceiver using photonic integrated circuit technology, which is designed to lower the overall cost of fiber to the home (FTTH) network installation.

iNEMI[7] estimates the current total telecom market at about $10 billion and growing steadily, with record quarters posted in 2008. Transceiver shipments grew from 40 million units in 2008 to 60 million units in 2012 for various market segments such as FTTH, Ethernet, fiber channel, Sonet/SDH, optical interconnects, and conventional/dense wavelength-division multiplexing. Overall, data transmission has grown at a CAGR of about 50% per year in recent years. Growth has been strongest in the Asia-Pacific region, with Europe, the Middle East, and Africa following, and North America stable. System companies are fairly healthy and are able to achieve over 50% gross margins, but component companies continue to struggle, with gross margins in the 20–30% range.

The entire transceiver/transponder market was estimated to be $2.1 billion in 2009, as shown in Figure A-2. The growth of bandwidth will require significant investments in new and expensive technologies like PLC/PIC, 25G, and lower cost VCSEL packaging.

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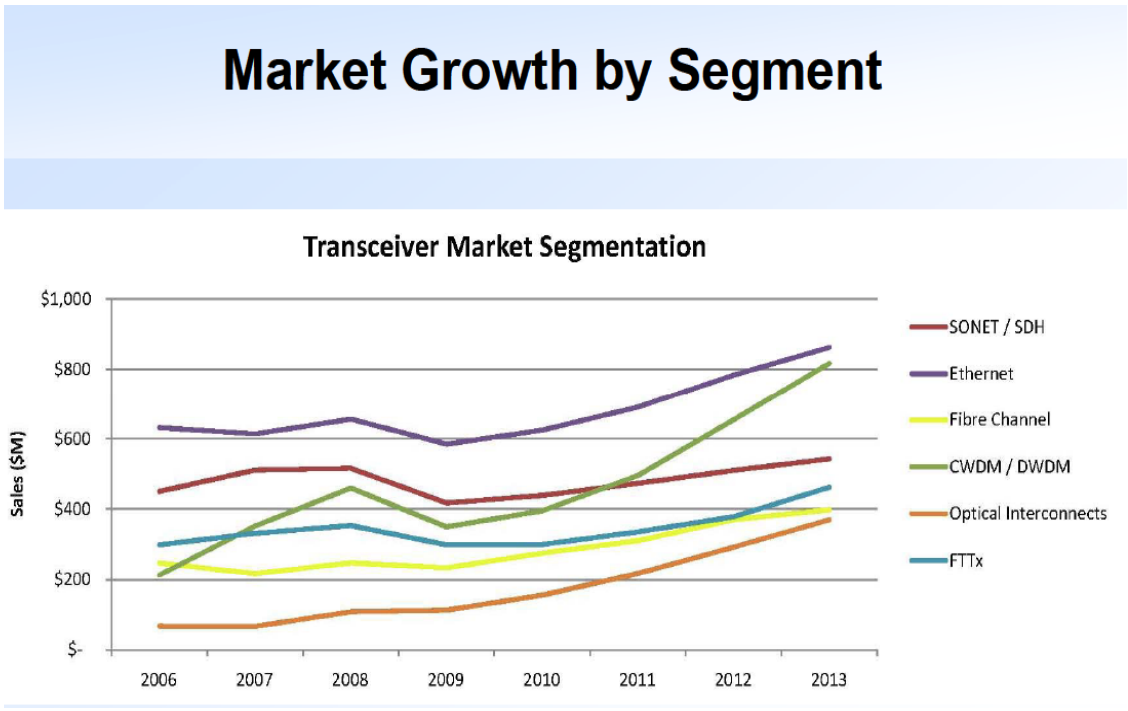
5 MarketsandMarkets, *Global Silicon Photonics Market (2010–2015)*, March 2011.

6 Research and Markets, *Photonic Integrated Circuit (IC) & Quantum Computing Market (2012–2022)*, December 2012.

7 iNEMI, *2013 Roadmap*.




Source: iNEMI, *2013 Roadmap*.

**Figure A-2. Transceiver Revenue by Major Market Segments Historically and as Forecast by LightCounting**

# Appendix B.
# Sustaining a Viable Foundry Ecosystem

A viable foundry ecosystem will require that sufficient runs can be regularly scheduled to maintain a minimum threshold of volume to meet some key constraints. Each run will host a certain number of projects using an MPW model, and each of those runs needs to be well utilized or costs will start to increase as space on each run is wasted.

## Number of Runs

An examination of ongoing runs at MOSIS suggests that most common processes have about 3–5 runs per year. When researchers utilize a run, they need to align their project timing to a particular run while leaving sufficient slack to ensure that they can complete their project on time. If runs are scheduled infrequently, this may cause researchers to have significant delays on their projects, which can be a problem, particularly for educational courses and graduate students. A rate of 3–5 runs per year would allow researchers to plan for fabrication with approximately 2–4 months maximum delay. Information from OpSIS recommends a cadence of 3–4 runs per year.[1] For the purposes of this analysis, we assumed that a foundry needs to have 3–4 runs at a minimum to support its users.

## Number of Projects on Each Run

A recent presentation by OPSIS noted that the typical reticles on its runs through IME were about 24×32 mm in size, a total area of 768 $mm^2$. A good target for utilization for a MPW run is 75%, which means that about 575 $mm^2$ in area should be utilized by projects. A limited sampling of projects found that at present, a number of projects were modest in size and used about 25 $mm^2$ in area. This size of 25 $mm^2$ is a common minimum size for many MOSIS runs. While we would expect that with advances, more complex projects would be built, at least at the beginning, MPWs may fit as many as 20–25 projects on a single run. OpSIS also confirms that 20–30 projects are typically on an MPW run. As more advanced projects are undertaken, the chips would be expected to be larger in area and over time MPWs may run with more like 10–15 projects on board.

[1] M. Hochberg, "OPSIS: Enabling a Transition from Devices to Systems," University of Washington, SEMICON west.

# Appendix C.
# Notable Global Capabilities in Silicon Photonics

This appendix provides a summary of selected global sources of silicon photonics fabrication and foundry services. It also lists some known global brokers who can arrange for MPW runs through the manufacturers. A more detailed list of global players can be found in Figure 7 in the main text.

The Institute of Microelectronics (IME)[1] was founded as a research institute of the Science and Engineering Research Council of the Agency for Science, Technology and Research (A*STAR) in 1991. Its objectives were to develop strategic competencies, enable technologically competition, and cultivate a technology talent pool in the Singapore's microelectronics industry. IME is one-stop-shop solution for low-cost prototyping and low-volume production for integrated circuits. It provides MPW services for 2.5D through silicon interposer and silicon photonics. It has capability to design, process, and integrate technology for packaging and assembly. IME has 200 mm and 300 mm engineering lines in a Class-10 cleanroom of 14,000 square feet. It has supported shared silicon photonics prototype runs with the option of using either IME's or a customer's own design, with the proviso that it be within technical specifications. This service allows academia and small companies to design systems without a large budget.

In September 2012, IME and MOSIS signed a memorandum of understanding to offer a multiproject wafer (MPW) service targeting silicon integrated photonics. The partnership specifically involves sharing costs for fabrication, reticles or masks, and the setup and use of the design environment. Photonics designers and researchers will also have access to IME's device library, which includes integrated active and passive devices. OpSIS also uses IME as a foundry.

Imec[2] is a nonprofit organization founded in 1984 to provide leading-edge research in the areas of nanoelectronics. Since its inception, Imec has offered a platform for application-specific design and process with the capabilities to do prototype, test, package,

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[1] A*STAR Institute of Microelectronics website, "Multi-Project Wafer (MPW) Services"; Solid State Technology website, "Singapore IME, MOSIS to Offer Silicon Photonics Wafer Prototyping Service," September 4, 2012.

[2] Imec website, "Imec Offers Fully Integrated Silicon Photonics Platform in a Multi-Project Wafer Service," Imec News, March 14, 2013.

and production runs on a 200 mm pilot line with 130 nm and 90 nm CMOS technologies. A joint initiative with LETI, where the advanced CMOS-compatible fabrication facilities can be used in photonic circuits, has led to the creation of the ePIXfab. Recently (March 2013) Imec announced the launch of its fully integrated silicon photonics platform through its MPW service via ePIXfab. The platform enables cost-effective R&D of silicon photonic ICs for high-performance optical transceivers (25 Gbps and beyond) and optical sensing and life-science applications. The offered integrated components include low-loss waveguides, efficient grating couplers, high-speed silicon electro-optic modulators, and high-speed germanium waveguide photo-detectors.

The Laboratoire d'électronique des technologies de l'information (LETI), a subsidiary of France's nuclear and renewable energy commission, is an advanced R&D center based in Grenoble, France. LETI has been involved with R&D in numerous high-technology areas, including photonics, and has an objective to provide capability for complete silicon photonics technology platform (design, process, test, and packaging) for photonics/electronics 3D integration on silicon. To accelerate adoption of silicon photonics technology for telecommunications and data communication sectors, LETI is focusing on the following:

- Establishing prototyping and manufacturing capabilities on 200 mm and 300 mm wafers.
- Designing and testing of silicon photonics components and links.
- Developing passive and active silicon components on silicon on insulator (SOI) substrates.
- Exploring new solutions for integrated photo-detectors and integrated emitter technologies (InP lasers, VCSELs).
- Exploring packaging solutions for the integration of CMOS electronics with SOI photonic-integrated circuits and for low-cost connections of dies to fibers.
- Heterogeneous integration of III-V on silicon.
  - Wafer-scale laser integration.
  - Wafer-scale testing.

LETI provides full-platform MPW shuttle for customers interested in realizing high-speed modulators, detectors, and multilevel passive devices through chips manufactured in 200 mm CMOS line.[3] LETI's full platform run is open for registration via ePIXfab with an option for packaging.

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[3] LETI website, "CEA–LETI Full Platform in MPW."

STMicroelectronics N.V. (ST) is a European semiconductor company that focuses on microelectronics and technologies for power, automotive, sensors, and embedded processing. ST's Crolles technology center in France currently has major CMOS R&D programs, including the value-added, derivative, high-performance analog BiCMOS technologies. In March 2012 STMicroelectronics announced an agreement to develop a 300 mm silicon photonics platform in collaboration with Luxtera Inc. using Luxtera's photonics technology.[4] This agreement will allow silicon/CMOS photonics specialist Luxtera to develop a dedicated silicon photonics process at its 300 mm research and pilot production wafer-fabrication process in ST CMOS 65 nm, 12-inch Crolles line (PIC25G) in France. Solutions for merged electronic/photonic products will be based on hybrid integration technology with CMOS dies through copper pillar technology. Production at Crolles would then enable the two companies to provide silicon photonics components and systems. The silicon photonics process will offer scalability of electro-optical transceivers for data rates of 100 Gbits per second, 400 Gbits per second, and beyond. It will support light at wavelengths of 1310 nm, 1490 nm, and 1550 nm. In turn, STMicroelectronics can now offer customers the world's leading optical IP as the two companies expand their silicon photonics ecosystem.

[4] P. Clark, "Luxtera, ST in deal to Take Silicon Photonics Mainstream," *EE Times*, March 1, 2012.

# Appendix D.
# Component Building Blocks of Photonic Integrated Circuits

1. **Waveguides**—a transmission medium for optical signals. Waveguide classification typically includes mode type (single-mode versus multimode) and material type (silicon on insulator, indium phosphide, silicon nitride).
    a. **Shallow Waveguide**—a waveguide that is simple to design and implement but only weakly confines the optical wave. Disadvantages include light leakage (optical loss per unit length) and high loss at waveguide bends due to weak horizontal confinement.
    b. **Deeply Etched Waveguide**—a waveguide that is more compact and confines the optical wave more completely. Typically has less bend loss. These waveguides are more difficult to fabricate than a shallow-etched design.
2. **Waveguide Crossing**—waveguide structure that allows crossing of signal paths with low crosstalk to control and direct the propagation of the light in a photonic integrated circuit. A multimode interference (MMI) based waveguide crossing features wavelength insensitivity and ease of design and fabrication.
3. **Y-Branch**—passive waveguide structure that splits the incoming optical signal into two paths while maintaining minimum loss due to reflection or radiation. Y-branches are theoretically lossless, but due to fabrication processes, sharp corners and rough surfaces can scatter a fraction of the optical signal.
4. **Couplers**—fiber to planar waveguide provides an interface between the optical fiber mode and waveguide modes. Coupler allows different connectors to connect with minimum loss and provides alignment for the optic signals.
    a. **Directional Coupler**—a 2×2 photonic switch that allows the signal to be switched from one channel to another or pass directly from input to output on the same channel under electrical control.
    b. **MMI Coupler**—offers large operation bandwidth, better manufacturing tolerances, and insensitivity to polarization. MMI couplers can be configured in 1×2, 2×2, and 4×4 modes.

c. **Single Polarization Grating Coupler**—consists of two sections, a horn-shape connecting waveguide and an extension of the horn-shape containing curved grating trenches that transform the incoming light from an optical fiber mode into a waveguide mode.

d. **Polarization Splitting Grating Coupler**—a coupler that splits the optical signal into two orthogonal polarizations and directs them to two separate waveguides where high-speed photodiodes are used to capture the individual polarized optical signals.

5. **Spot-Size Converter**—a single-channel input-output component that enable direct coupling of waveguides without causing compatibilities issues (e.g., different mode sizing).

6. **Modulator**—a device used to encode information. Optical modulation can be implemented by changing the optical intensity via absorption, or changing the refractive index of the material.

   a. **Electro-Optical Modulator**—electrically controls the amplitude, phase, and polarization state of a light source. Current preferred material in electro-optical modulator is ferroelectric due to optical transparency, thermal and temporal stability.

   b. **Thermo-Optic Modulator**—exploits the thermal dependence of refractive index via local heater-induced temperature to tune modulation optical resonators.

   c. **Carrier-Injection Modulator**—can be either metal-oxide-semiconductor capacitors or p-i-n diodes. Induced charge can provide large changes in the refraction index and realize high modulation depths in submicron devices.

7. **Ring Resonator**—a waveguide that forms a closed loop or “ring.” Ring resonators are useful when coupled to an optical network as they will behave as a spectral filter.

8. **Arrayed Waveguide Grating (AWG)**—used as optical multiplexers, the devices are able to disperse multiple wavelengths propagating in a single waveguide into multiple, spatially separated output waveguides or vice versa. AWG is used in systems that employ wavelength division multiplexing.

9. **Distributed Bragg Reflector (DBR)**—a mirror structure formed by etching a grating (wavelength selective element) in a one-dimensional waveguide or by alternating a sequence of layers of two different optical materials in a two-dimensional structure. DBR is a key wavelength selective element used in the fabrication of lasers for wider variety of emission wavelengths and higher quality values.

10. **Semiconductor Optical Amplifier (SOA)**—a semiconductor laser waveguide structure without feedback that can provide optical amplification. SOAs are polarization insensitive such that the input light will be amplified regardless of the polarization type.
11. **Photodiode**—a type of photodetector that is able to convert light into a current or voltage source. Photodiodes operate by generating charge through absorption of photons to generate a flow of current in an external circuit.
    a. **Balanced Photodiode**—a pair of photodiodes balanced to allow better signal-to-noise ratio.

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# Abbreviations

| | |
|---|---|
| 3D | three-dimensional |
| A*STAR | Agency for Science, Technology and Research |
| ASIC | application-specific integrated circuit |
| AWG | Arrayed Waveguide Grating |
| CAD | computer-aided design |
| CAGR | compound annual growth rate |
| CAPEX | Capital Expenditure |
| CMOS | Complementary metal-oxide semiconductor |
| DARPA | Defense Advanced Research Projects Agency |
| DBR | Distributed Bragg Reflector |
| EDA | electronic design automation |
| EPIC | European Photonics Industry Consortium |
| FTTH | fiber to the home |
| Gbps | gigabits per second |
| IC | integrated circuit |
| IDA | Institute for Defense Analyses |
| IDM | integrated device manufacturer |
| IME | Institute of Microelectronics |
| iNEMI | International Electronics Manufacturing Initiative |
| InP | indium phosphide |
| IP | intellectual property |
| LETI | Laboratoire d'électronique des technologies de l'information |
| MEMS | microelectormechanical systems |
| MMI | multimode interference |
| MOS | metal-oxide semiconductor |
| MOSIS | Metal Oxide Semiconductor Implementation Service |
| MPW | multiproject wafer |
| nm | nanometer |
| NSF | National Science Foundation |
| OIDA | Optoelectronics Industry Association |
| PDK | process design kit |
| PIC | photonic integrated circuit |
| SBIR | Small Business Innovative Research |
| Si | silicon |
| SOA | Semiconductor Optical Amplifier |
| SOI | silicon on insulator |
| ST | STMicroelectronics N.V. |
| STPI | Science and Technology Policy Institute |
| VCSEL | vertical-cavity surface-emitting laser |

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Advances in photonics technology are simultaneously improving the performance and reducing the size and power of important communication, computing, and sensing capabilities. Innovation in the application of photonics technology is an important pillar of competitiveness in important areas of interest to the nation and to national security. The objective of this project was to survey available concepts for how to employ a photonics foundry to enable an innovative ecosystem for advanced integrated optics and electronics. This report provides background, summarizes analyses, identifies gaps, and provides a roadmap and resourcing for the foundry concept.

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